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VLSI-design of reconfigurable logic blockbased sequential circuits using Look-up table logics

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Abstract:

The advancement of Very-Large-Scale Integration (VLSI) technology has made it possible to create highly efficient sequential circuits, such as counters and shift registers, utilizing reconfigurable logic blocks. Statistics show that by 2026, the global VLSI market is projected to reach approximately $50 billion, driven by the demand for versatile and adaptive electronic components in various applications. Traditional logic gate-based sequential circuits often suffer from inflexibility and high resource consumption, leading to inefficiencies in design and performance, particularly in dynamic environments where rapid reconfiguration is required.

This paper proposes a novel approach to designing sequential circuits based on reconfigurable logic blocks using lookup table (LUT) logic. By employing LUT-based architectures, the proposed counters and shift registers achieve greater adaptability and lower power consumption compared to conventional designs. The utilization of LUTs allows for efficient implementation of complex logic functions while simplifying the overall design process. This innovation not only enhances performance metrics such as speed and power efficiency but also facilitates faster prototyping and testing in VLSI front-end design. The resulting reconfigurable logic blocks offer a significant contribution to the design landscape, making it easier to meet the diverse requirements of modern electronic applications.

Keywords: VLSI design, LUT-based architecture
Reconfigurable circuits, Sequential logic design
Low-power circuits, High-speed design
Logic optimization, Digital circuit prototyping
Adaptive electronics, FPGA-based design

1. INTRODUCTION

Sequential circuits are digital circuits that store and use the previous state information to determine their next state. Unlike combinational circuits, which only depend on the current input values to produce outputs, sequential circuits depend on both the current inputs and the previous state stored in memory elements. Sequential circuits are commonly used in digital systems to implement state machines, timers, counters, and memory elements. The memory elements in sequential circuits can be implemented using flip-flops, which are circuits that store binary values and maintain their state even when the inputs change. There are two types of sequential circuits: Asynchronous and Synchronous sequential circuits.

Asynchronous Sequential Circuit: These circuits **do not use a clock signal** but uses the pulses of the inputs as shown in Figure 1.1. These circuits are **faster** than synchronous sequential circuits because there is clock pulse and change their state immediately when there is a change in the input signal. We use asynchronous sequential circuits when speed of operation is important and **independent** of internal clock pulse. But these circuits are more difficult to design and their output is uncertain.

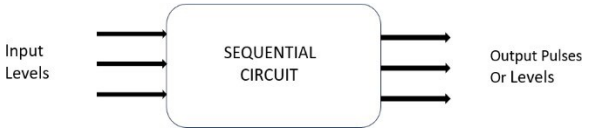

Figure: 1.1 Asynchronous Sequential Circuit

Synchronous Sequential Circuit: These circuits **use clock signal** and level inputs (or pulsed) (with restrictions on pulse width and circuit propagation) as shown in Figure 1.2. The output pulse is the same duration as the clock pulse for the clocked sequential circuits. Since they wait for the next clock pulse to arrive to perform the next operation, so these circuits are bit **slower** compared to asynchronous. Level output changes state at the start of an input pulse and remains in that until the next input or clock pulse.

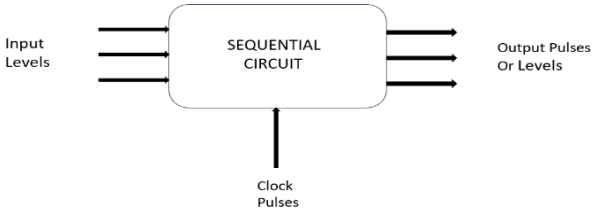

Figure: 1.2 Synchronous Sequential Circuit

1.2 Research Motivation

Figure 3.1 shows the reconfigurable logic block based sequential circuit. In this block diagram the first block contains sequential circuits are a type of digital circuit in which the output depends not only on the current inputs but also on the past sequence of inputs. These circuits have memory elements, typically in the form of flip-flops, to store information about previous inputs and outputs.

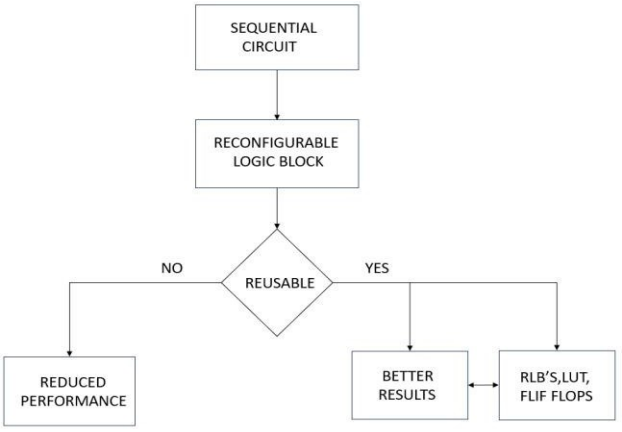

Figure: 1.3 Research Motivation

The preceding block mentions that the reconfigurable logic blocks are programmable, adaptable, and dynamic in nature. These blocks are fundamental components in reconfigurable devices, such as

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Field-Programmable Gate Arrays (FPGAs). These blocks provide a level of flexibility and programmability that allows users to configure the hardware for specific tasks or applications. If the reconfigurable logic block incorporates reusability, the system performance is enhanced; otherwise, the absence of this property may lead to a decline in performance.

2. LITERATURE SURVEY

[1] Sanadhya, et al. developed a power optimization method for battery-powered digital circuits using adiabatic logic. This approach reduces power dissipation by slowing logic transitions and improving energy efficiency in VLSI circuits. Various adiabatic techniques were analyzed for combinational and sequential circuits, showing better performance than traditional methods.

[2] Govindaraj, et al. proposed a low-power test pattern generator (TPG) using LFSR and binary ripple counter to minimize dynamic power consumption during VLSI circuit testing. Their approach increased the correlation between successive test vectors, significantly reducing power dissipation in test mode.

[3] Pomeranz, et al. suggested an iterative synthesis method to improve VLSI design parameters and detect undetectable faults efficiently. Their approach prevents a decrease in fault coverage by identifying and eliminating ineffective design modifications in test generation.

[4] Angadi, et al. developed a built-in self-test (BIST) architecture for combinational logic circuit verification. Using LFSR-based test patterns, the proposed method effectively detects errors in circuits while minimizing hardware complexity, making testing more efficient and cost-effective.

[5] Chandra, et al. focused on low-power VLSI design strategies, particularly optimizing adders for better power and area efficiency. They proposed a ripple carry adder using full swing gate diffusion input technology to reduce size, power, and complexity in digital circuits.

[6] Priyadarshini, et al. designed a novel D Flip Flop (DFF) using supply voltage techniques to lower leakage power consumption. Their method reduces power dissipation in standby mode while employing fewer transistors, improving efficiency in CMOS-based digital designs.

[7] Minakshi, et al. proposed a D Flip Flop using direct current diode-based positive feedback adiabatic logic (DC-DB PFAL) to reduce power dissipation. Their analysis at various frequencies showed an 18% improvement in power efficiency with fewer transistors than existing designs.

[8] Shah, et al. introduced a sense amplifier-based flip flop (SAFF) for high-speed and low-power applications. The proposed flip flop achieves significant power reduction, glitch-free operation, and improved speed, making it suitable for high-performance VLSI circuits.

[9] Yinghua, et al. developed an FC-guided SAT-based attack to break combinational and sequential logic locking efficiently. Their approach significantly speeds up key retrieval in logic encryption, reducing SAT-solving time by up to 90× compared to previous attacks.

[10] Ramakrishnan, et al. explored reversible logic for low-power combinational and sequential circuits. Their MGDI-based approach minimizes power consumption, transistor count, and propagation delay while maintaining logic simplicity, enhancing VLSI circuit design.

[11] Harikrishna, et al. designed a low-power square root calculator using reversible logic and a non-restoring algorithm. The binary square rooter, implemented using RCSM and SRG gates, reduces hardware resources while maintaining efficient power consumption.

[12] Nousheen, et al. proposed a hardware-oriented image compression algorithm for wireless sensor networks. Their approach integrates fuzzy decision-making, block partitioning, and Huffman coding, achieving high compression ratios while maintaining low power consumption.

[13] Geonhwi, et al. developed a high-speed, low-power synchronous up/down counter using a compact toggle flip-flop. Their design improves counting speed by 55% and reduces power-delay product by 28%, enhancing energy-efficient VLSI designs.

[14] Moraitis, et al. surveyed FPGA security threats and bitstream modification attacks. They discussed existing protection mechanisms, potential vulnerabilities, and countermeasures to ensure FPGA-based systems' security in critical applications.

[15] Irith, et al. introduced a test data compression method for scan-based testing, reducing test sequence length. Their approach enables efficient on-chip decompression, minimizing test data storage requirements while maintaining fault coverage.

3. PROPOSED METHODOLOGY

Counters in digital circuits are fundamental components used to generate sequences of binary numbers. They are widely employed in various applications such as frequency division, digital clocks, event counting, and addressing memory locations. Counters can be synchronous or asynchronous and come in different types such as binary counters, BCD (Binary-Coded Decimal) counters, and asynchronous counters. In VLSI, counters are digital circuits used to count events or sequences of events. They are widely used in various applications such as frequency synthesis, digital signal processing, and timing generation. Counters can be classified based on their type (e.g., binary, BCD, asynchronous, synchronous), counting direction (up or down), and triggering mechanism (e.g., synchronous or asynchronous).

Types of Shift Registers

- Serial-in Serial-out (SISO): Data is entered serially at one end and shifted out serially at the other end.
- Serial-in Parallel-out (SIPO): Data is entered serially and output in parallel.
- Parallel-in Serial-out (PISO): Data is entered in parallel and shifted out serially.
- Parallel-in Parallel-out (PIPO): Data is entered and output in parallel.

Shift registers in VLSI refer to the implementation of shift registers using integrated circuit technology, typically using CMOS (Complementary Metal-Oxide-Semiconductor) fabrication processes. In VLSI design, shift registers are often optimized for

area, speed, and power efficiency to meet the requirements of modern digital systems. Overall, shift registers play a crucial role in VLSI design, enabling the implementation of various digital functionalities in modern integrated circuits.

Proposed Counter

The above figure 4.1 shows proposed architecture for scan FF inserted bidirectional counters.

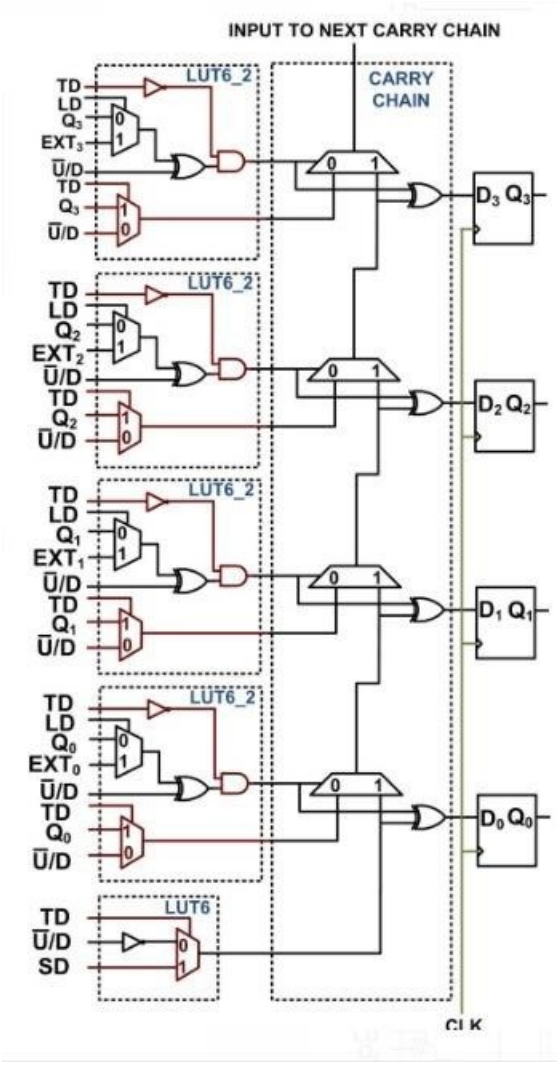

Figure: 4.1 proposed architecture for scan FF inserted bidirectional counters

LUT

In VLSI, a LUT (Look-Up Table) is a fundamental component used in digital logic design. It's essentially a small, programmable memory unit that stores output values for all possible input combinations. LUTs are commonly used in FPGA (Field-Programmable Gate Array) designs to implement logic functions and to perform tasks such as signal processing, arithmetic operations, and data manipulation. They provide flexibility and efficiency in implementing complex logic functions by allowing designers to define custom logic without the need for dedicated hardware.

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2-to-1 multiplexer

A 2-to-1 multiplexer (mux) is a fundamental component in digital circuits that selects between two input signals based on a control signal. Its operation is crucial for data selection and routing in various electronic devices, ranging from simple integrated circuits to complex computer systems. Let's delve into the detailed operation of a 2-to-1 multiplexer.

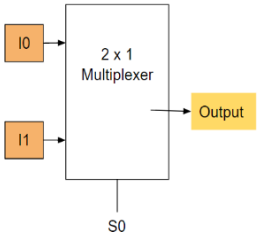

Figure 4.2. Multiplexer 2*1

Inputs		S0	Output
I0	I1		
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	1

Table 4.2. Multiplexer 2*1

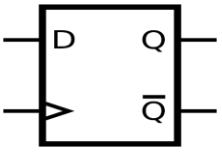

Figure 4.3. D-Flip Flop Without CE

D	Q	$\bar{Q}$
0	Q	0
1	Q	1

Table 4.3. D-Flip Flop Without CE

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Proposed Shift registers

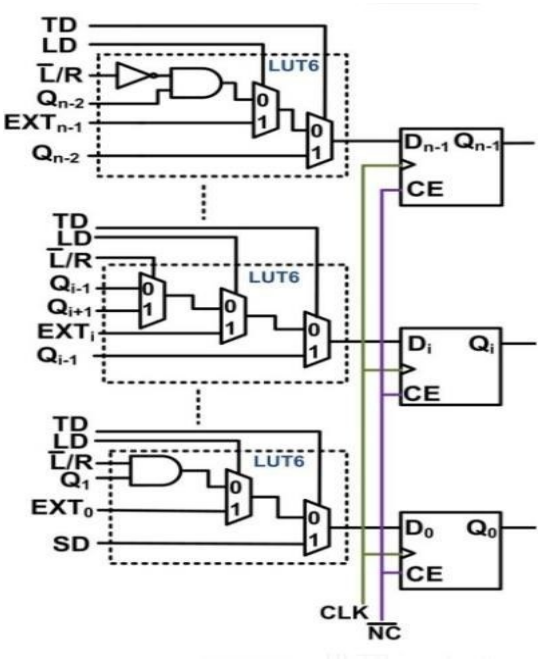

Figure 4.4. Proposed architecture for scan FF inserted Universal Shift Register

D-Flip Flop With CE

A D flip-flop with a clock enable (CE) input is a digital storage device that holds one bit of data. In addition to the data input (D), it features a clock enable input (CE) which determines when the flip-flop is allowed to change its state. When the clock enable signal is high, the flip-flop operates as normal, capturing the input data on the rising or falling edge of the clock signal.

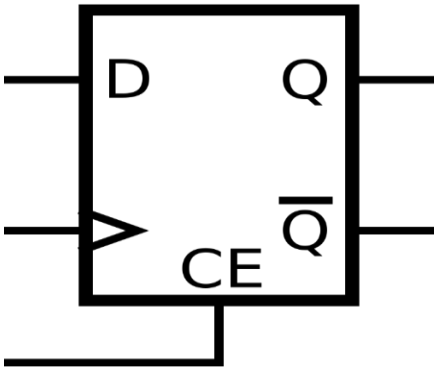

Figure 4.3. D-Flip Flop With CE

D	CLK	CE	Q	$\bar{Q}$
0	1	0	Q	Q
1	1	0	Q	Q
0	1	1	Q	0
1	1	1	Q	1

Table 4.3. D- Flip Flop With CE

4 . EXPERIMENTAL ANALYSIS.

Existing Counter

Figure 6.1. Existing Simulation Results for N=32

Figure 6.2 shows existing area measurements for N=32. Here, 1286 number of LUT's are used out of Available 133800 LUT's which consumes 0.96% of utilization, 32 number of FF's are used out of Available 267600 FF's which consumes 0.01% of utilization, 6 number of DSP's are used out of Available 740 DSP's which consumes 0.81% of utilization, 69 number of IO's are used out of Available 500 IO's which consumes 13.80% of utilization, 1 number of BUFG's are used out of Available 32 BUFG's which consumes 3.13% of utilization

Resource	Utilization	Available	Utilization %
LUT	1286	133800	0.96
FF	32	267600	0.01
DSP	6	740	0.81
IO	69	500	13.80
BUFG	1	32	3.13

Figure 6.2. Existing Area for N=32

Figure 6.3 shows existing Setup delay for N=32. Here, maximum Total Delay is 113.892 ns, maximum Logic Delay is 58.494 ns, maximum Net Delay is 55.397 ns.

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Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To
Path 1	∞	206	174	62	next_count1_reg[1]/C	next_count1_re
Path 2	∞	197	166	62	next_count1_reg[1]/C	next_count1_re
Path 3	∞	188	158	62	next_count1_reg[1]/C	next_count1_re
Path 4	∞	179	150	62	next_count1_reg[1]/C	next_count1_re
Path 5	∞	170	142	62	next_count1_reg[1]/C	next_count1_re
Path 6	∞	161	134	60	next_count1_reg[1]/C	next_count1_re
Path 7	∞	152	126	58	next_count1_reg[1]/C	next_count1_re
Path 8	∞	143	118	56	next_count1_reg[1]/C	next_count1_re
Path 9	∞	134	110	54	next_count1_reg[1]/C	next_count1_re
Path 10	∞	126	103	52	next_count1_reg[1]/C	next_count1_re

Figure 6.3 Existing Setup Delay for N=32

Figure 6.4 shows existing Hold delay for N=32. Here, maximum Total Delay is 1.107 ns, maximum Logic Delay is 0.664 ns, maximum Net Delay is 0.596 ns.

Unconstrained Paths - NONE - NONE - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 11	∞	2	1	5	next_count1_reg[0]/C	next_count1_reg[0]/D	0.488	0.255	0.233	-∞	
Path 12	∞	4	2	4	next_count1_reg[5]/C	next_count1_reg[6]/D	0.911	0.531	0.380	-∞	
Path 13	∞	4	2	4	next_count1_reg[4]/C	next_count1_reg[4]/D	0.943	0.487	0.456	-∞	
Path 14	∞	4	2	4	next_count1_reg[5]/C	next_count1_reg[8]/D	0.953	0.616	0.337	-∞	
Path 15	∞	4	2	4	next_count1_reg[5]/C	next_count1_reg[5]/D	0.984	0.487	0.497	-∞	
Path 16	∞	3	2	4	next_count1_reg[2]/C	next_count1_reg[3]/D	1.034	0.559	0.475	-∞	
Path 17	∞	3	2	4	next_count1_reg[30]/C	next_count1_reg[31]/D	1.056	0.533	0.523	-∞	
Path 18	∞	4	2	4	next_count1_reg[22]/C	next_count1_reg[22]/D	1.072	0.476	0.596	-∞	
Path 19	∞	5	3	4	next_count1_reg[5]/C	next_count1_reg[9]/D	1.075	0.664	0.411	-∞	
Path 20	∞	4	2	4	next_count1_reg[17]/C	next_count1_reg[20]/D	1.107	0.616	0.491	-∞	

Figure 6.4 Existing Hold Delay for N=32

Figure 6.5 shows existing power measurements for N=32. Here, the total power is 50.754 W, Static power includes PL Static power of 0.586 W, Dynamic power includes signal power of 11.076 W, Logic power of 11.203 W, DSP power of 2.433 and I/O power of 25.456 W.

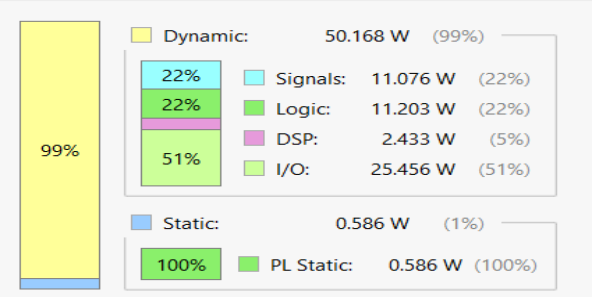

Figure 6.5 Existing power for N=32

6.2 Proposed Counter

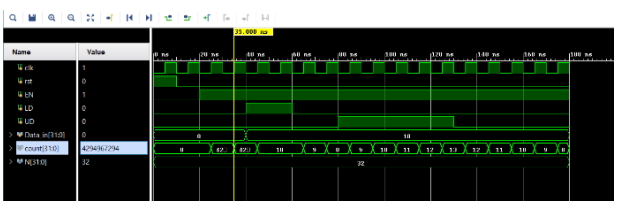

Figure 6.6 Proposed Counter Results for N=32

Figure 6.7 shows proposed area measurements for N=32. Here, 32 number of LUT's are used out of Available 133800 LUT's which consumes 0.02% of utilization, 32 number of FF's are used out of Available 267600 FF's which consumes 0.01% of utilization, 69 number of IO's are used out of Available 500 IO's which consumes 13.80% of utilization, 1 number of BUFG's are used out of Available 32 BUFG's which consumes 3.13% of utilization.

Resource	Utilization	Available	Utilization %
LUT	32	133800	0.02
FF	32	267600	0.01
IO	69	500	13.80
BUFG	1	32	3.13

Figure 6.7 Existing Area for N=32

Figure 6.8 shows proposed Setup delay for N=32. Here, maximum Total Delay is 12.185 ns, maximum Logic Delay is 3.439 ns, maximum Net Delay is 8.754 ns.

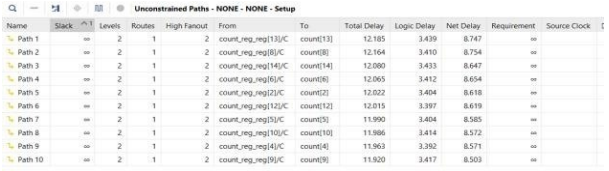

Figure 6.8 Proposed Setup Delay for N=32

Figure 6.9 shows proposed Hold delay for N=32. Here, maximum Total Delay is 0.599 ns, maximum Logic Delay is 0.349 ns, maximum Net Delay is 0.250 ns.

Figure 6.9 Proposed Hold Delay for N=32

Figure 6.10 shows proposed power measurements for N=32. Here, the total power is 25.182 W, Static power includes PL Static power of 0.211 W, Dynamic power includes signal power of 1.351 W, Logic power of 0.259 W and I/O power of 23.361 W

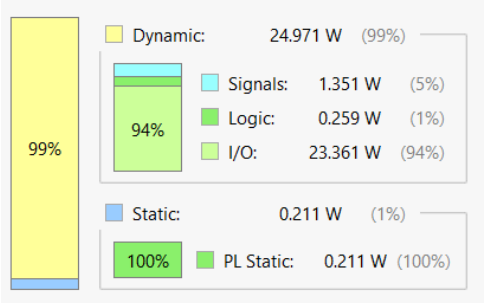

Figure 6.10 Proposed power for N=32

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6.3 Existing Shift Register

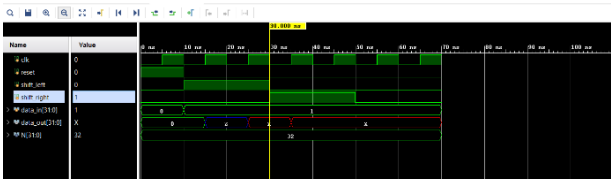

Figure 6.11 Existing Shift Register Result for N=32

Figure 6.12 shows existing area measurements for N=32. Here, 540 number of LUT's are used out of Available 133800 LUT's which consumes 0.40% of utilization, 28 number of FF's are used out of Available 267600 FF's which consumes 0.01% of utilization, 3 number of DSP's are used out of Available 740 DSP's which consumes 0.41% of utilization, 68 number of IO's are used out of Available 500 IO's which consumes 13.60% of utilization, 1 number of BUFG's are used out of Available 32 BUFG's which consumes 3.13% of utilization.

Resource	Utilization	Available	Utilization %
LUT	540	133800	0.40
FF	28	267600	0.01
DSP	3	740	0.41
IO	68	500	13.60
BUFG	1	32	3.13

Figure 6.12 Existing Area for N=32

Figure 6.13 shows existing Setup delay for N=32. Here, maximum Total Delay is 104.452 ns, maximum Logic Delay is 51.841 ns, maximum Net Delay is 52.610 ns.

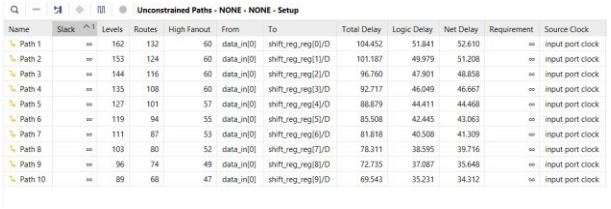

Figure 6.13 Existing Setup Delay for N=32

Figure 6.14 shows existing Hold delay for N=32. Here, maximum Total Delay is 1.254 ns, maximum Logic Delay is 0.531 ns, maximum Net Delay is 0.772 ns.

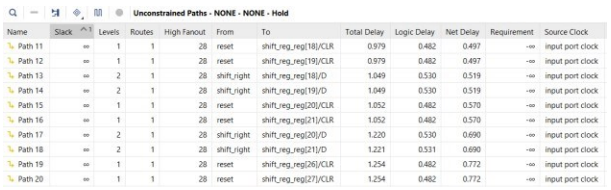

Figure 6.14 Existing Hold Delay for N=32

Figure 6.15 shows existing power measurements for N=32. Here, the total power is 17.635 W, Static power includes PL Static power of 0.168 W, Dynamic power includes signals power of 4.521 W, Logic power of 4.854 W, DSP power of 1.012 W and I/O power of 7.081 W.

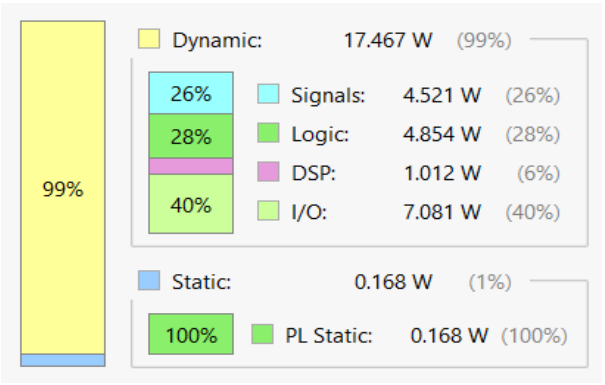

Figure 6.15 Existing power for N=32

6.4 Proposed Shift Register

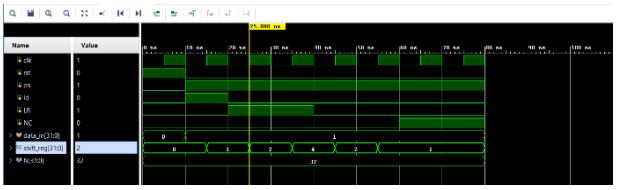

Figure 6.16 Proposed Simulation Result for N=32

Figure 6.17 shows proposed area measurements for N=32. Here, 33 number of LUT's are used out of Available 133800 LUT's which consumes 0.02% of utilization, 32 number of FF's are used out of Available 267600 FF's which consumes 0.01% of utilization, 70 number of IO's are used out of Available 500 IO's which consumes 14.00% of utilization, 1 number of BUFG's are used out of Available 32 BUFG's which consumes 3.13% of utilization.

Resource	Utilization	Available	Utilization %
LUT	33	133800	0.02
FF	32	267600	0.01
IO	70	500	14.00
BUFG	1	32	3.13

Figure 6.17 Existing Area for N=32

Figure 6.18 shows proposed Setup delay for N=32. Here, maximum Total Delay is 6.599 ns, maximum Logic Delay is 3.380 ns, maximum Net Delay is 5.381 ns.

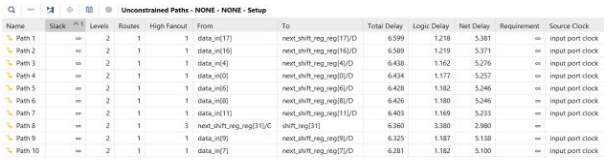

Figure 6.18 Proposed Setup Delay for N=32

Figure 6.19 shows proposed Hold delay for N=32. Here, maximum Total Delay is 0.454 ns, maximum Logic Delay is 0.255 ns, maximum Net Delay is 0.199 ns.

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Figure 6.19 Proposed Hold Delay for N=32

Figure 6.20 shows proposed power measurements for N=32. Here, the total power is 6.192 W, Static power includes PL Static power of 0.131 W, Dynamic power includes signal power of 0.521 W, Logic power of 0.099 W and I/O power of 5.441 W.

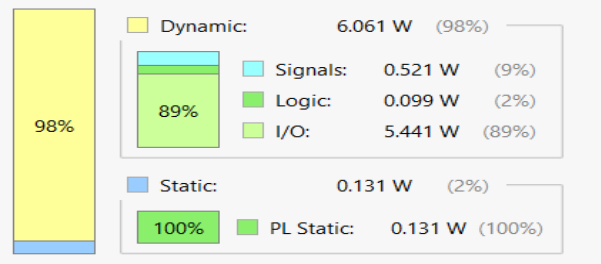

Figure 6.20 Proposed power for N=32

5 . CONCLUSION

In designing reconfigurable logic block-based sequential circuits, we have significantly reduced the number of lookup tables, leading to improvements in area, power consumption, and delay. Our proposed counter uses only 32 lookup tables, compared to 1286 in the existing design, cutting power usage to 25% and reducing delay. Similarly, our shift register design requires just 33 lookup tables, a major reduction from 540, and consumes only 6% of the power, with lower delay. These innovations result in more efficient and high-performance counters and shift registers.

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